The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because e.g. they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

Applicant gratefully acknowledges the Office Action's indication that claims 1, 4, 20 and 21 are allowed.

I. CLAIMS 12 AND 22-29 SATISFY THE REQUIREMENTS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The Office Action rejects claims 12 and 22-29 under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification. This rejection is respectfully traversed.

Specifically, the Office Action asserts that the specification never disclosed an impurity concentration of the channel region (215) is equal to an impurity concentration in the drift region (214), and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region as claimed in claim 12. This and other assertions are respectfully traversed.

As discussed during the interview, the specification does disclose that an impurity concentration contained in the channel is set equal to or less than the impurity concentration in the n drift region 114 (page 8, lines 18-19). Accordingly, the claimed feature "the impurity

not OK

fig. 9B

concentration contained in the channel (215) is set equal to or less than the impurity concentration in the n drift region (214)" is inherent in the specification. See, also, specification page 9, lines 25-29.

Regarding claims 24 and 25, the Schottky junction with the chemical region is disclosed at least at page 7, lines 12-14 with Fig. 7. The specification disclosed that the second embodiment differs from the above-mentioned first embodiment in substrate and conductive type at page 8, lines 15-16. Thus, "at least a part of the source electrode forms a Schottky junction with the channel region (215)" is inherent in the specification. For example, the specification at page 9, lines 31-32 discloses that the fourth embodiment is a Schottky diode, and that it is also possible to use the P-type channel region.

Regarding claim 26, the specification discloses that an n+-type extension region 100 and an insulating layer 24 may be provided on the n+-type region 20 for contact with the source electrode 22 at page 7, lines 21-22. Therefore, the features of claim 26 are inherent in the specification. However, claim 26 is amended to comport with Fig. 8, and thus obviate the claim rejection.

For at least these reasons, Applicant respectfully asserts that claims 12 and 22-29 are fully supported in the specification. Accordingly, withdrawal of the rejection of claims 12 and 22-29 under 35 U.S.C. §112, first paragraph, is respectfully requested.

II. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 12 and 22 under 35 U.S.C. §102(e) over U.S. Patent 5,998,834 to Williams et al. (hereinafter "834 Williams"); claim 23 under 35 U.S.C. §103(a) over the 834 patent; and claim 30 under 35 U.S.C. §102(b) over U.S. Patent No. 5,661,322 to Williams et al. (hereinafter the "322 Williams"). These rejections are respectfully traversed.

834 Williams does not teach, disclose or suggest "a source region having the first conductive type and provided on the channel region, the source region is located substantially

at a center of the channel region, and the source region is isolated from the insulation film," as recited in claim 12. Rather, Figure 10 of 834 Williams shows the source region 106 abutting the oxide layer 105 on all sides.

Claim 30 is now amended to recite the features of "first cathode region having a first conductive type; second cathode region having the first conductive type ... a first anode region having a second conductive type ... a trench structure ... and a second anode region having the second conductive type ..., wherein an impurity concentration in the first anode region is equal to or less than an impurity concentration in the second cathode region." 322 Williams does not teach, disclose or suggest the above recited claim features.

Instead, 322 Williams shows MOSFET layers having a common conductive type.

For at least these reasons, it is respectfully submitted that claims 12 and 30 are patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Applicant respectfully requests that the rejections under 35 U.S.C. §102(e), §103(a) and §102(b) be withdrawn.

III. CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 4, 12 and 20-30 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

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JAO:RJK/mdw

Date: March 10, 2003

Attachment:
Appendix

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Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

12. (Six Times Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a second conductive type different from the first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the first conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film, wherein an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.

26. (Twice Amended) The semiconductor device according to claim ~~12~~ 1, further comprising a semiconductor layer having the second ~~first~~ conductive type located between the source region and the source electrode, the semiconductor layer including an end face extended to a position covering at least a portion of the gate region.

30. (Three Times Amended) A semiconductor device comprising:

a ~~substrate~~ first cathode region having a first conductive type;

a ~~drift~~ second cathode region having the first conductive type and disposed on the ~~substrate~~ first cathode region;

a ~~channel~~ first anode region having a ~~first~~ second conductive type and provided on the ~~drift~~ second cathode region; ~~and~~

a ~~gate region~~ trench structure provided so as to surround at least the ~~channel~~ first anode region via an insulation film~~,~~; and

a second anode region having the second conductive type and provided on the first anode region, wherein an impurity concentration in the ~~channel~~ first anode region is equal to or less than an impurity concentration in the ~~drift~~ second cathode ~~region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region~~.